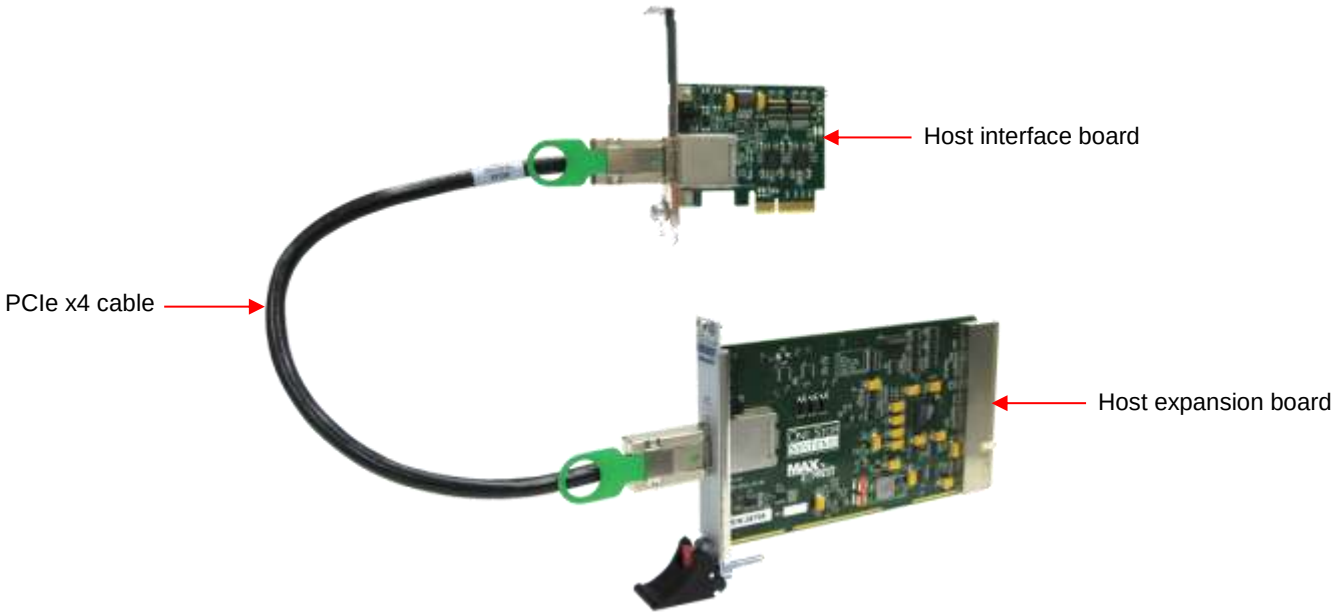
User Manual,
PCIe x4 Host Cable Adapter (HIB2)

OSS-KIT-EXP-4500

Table of Contents

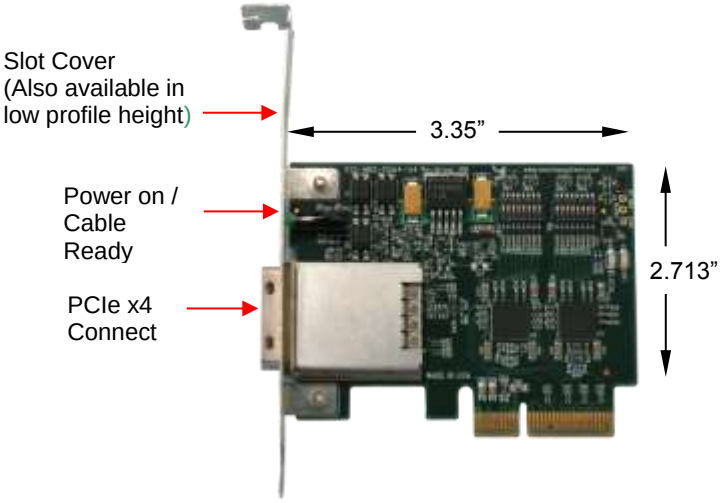
1.a. Description

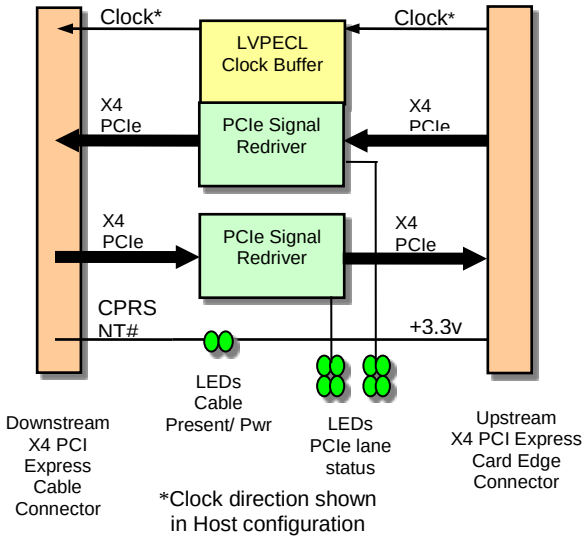
The Host Interface Board (HIB2) sits in the host machine and cables to the Host Expansion Board (HEB2). The Host Expansion Board site in a CPCI/CPCE Chassis.



1.b. Host interface board

The PCIe x4 host Interface board installs in a PCIe x4, x8, or x16 PCIe slot of a host system and cables down to a PCIe expansion system or other PCIe x4 device.

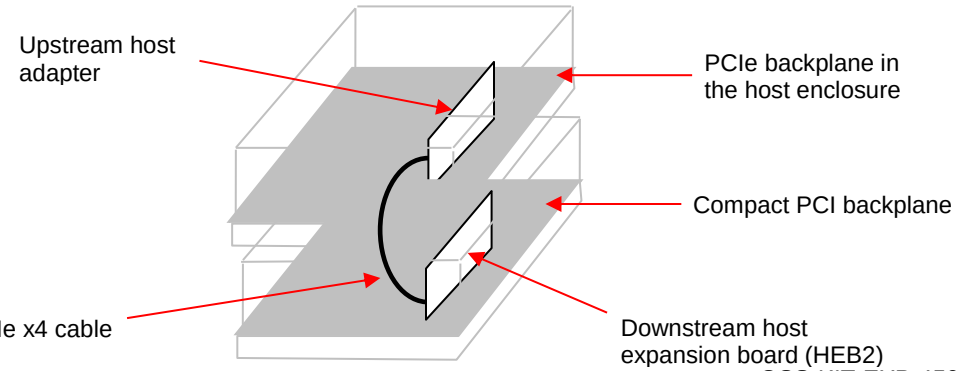




1.c. Host Expansion Board

The Host Expansion Board (HEB2) fits into the system slot of the CPCI chassis and connects through a high-speed PCIe x4 cable to an upstream host. The HEB2 expands the PCI Express bus from a PCIe slot to a CompactPCI system at 20Gb/sec.

1.d. Conceptual architecture



2 Specifications

2.a. Host interface board specifications

Electrical/Mechanical Specifications	
Form Factor:	ExpressCard/34
Dimensions (H x L):	1.34 x 5.01 inches (34 x 127.3mm)
External Connectors:	One PCIe x4 cable connector
Board Indicators:	Power On / Cable Present LEDs
Power Consumption (designed to meet the following conditions	
	3W typical, 3.3V@1A
Operating Environment (designed to meet the following conditions)	
Temperature Range:	0° to 55°C (32° to 131°F)
Relative Humidity:	10 to 90% non-condensing
Shock:	30g acceleration peak (11ms pulse) no cable connected
Vibration:	5-17 Hz 0.5” double amplitude displacement; 7-2000Hz, 1.5g acceleration.
Redriver	
Pericom PIEQX4401	
Agency Compliance Designed to meet, but not tested	
	UL60950, FCC Class B, CE safety and emissions

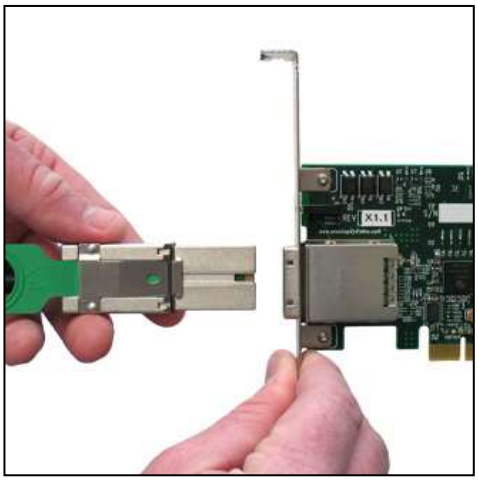
2.b. Host expansion board specifications

CPCI Interface	• 32 or 64 bit at 66 or 33MHz • 3.3V I/O only • Internal arbiter supports up to 4 external masters • Seven CPCI slots (up to 7 PCI clock/bus requests) • Enhanced Intel SpeedStep Technology
Cable Interface	• Single port x4 link width • 100MHz reference clock • 256 byte maximum payload size • Automatic link training (auto-negotiate to largest common width) • Advance flow control, CRC and error reporting • Molex 75586-0010 connector
Electrical/Mechanical	• 3U or 6U CPCI system master or peripheral slot • 3U [H x L x W] dimensions of 3.937 x 6.299 x 0.6” (100 x 160 x 1.6mm) • Tundra Tsi384 • 32/64-Bit/33/66MHz CPCI bus on connectors J1 & J2 • Four green front panel indicators • Automatic downstream select cable dip switches
Operating Environment	• Temperature range 0 to 50C (32 to 122F) • Relative Humidity 5 to 90% non-condensing • Shock: 5-17 Hz 0.5” double amplitude displacement; 7-2000Hz, 1.5g acceleration
Agency Compliance:	+*Designed to meet UL 60950, FCC Class B, CE safety and emissions*

3. Installation Instructions

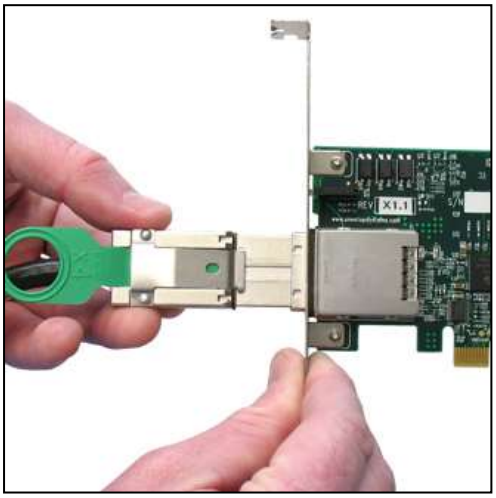
3.a. Connecting PCIe cable

1) To install the PCIe cable, Insert into the expansion link board firmly or until you feel it lock into place.



3.b. Removing PCIe cable:

1) To remove PCIe cable pull back on green thumb tab to release metal pins and gently separate.

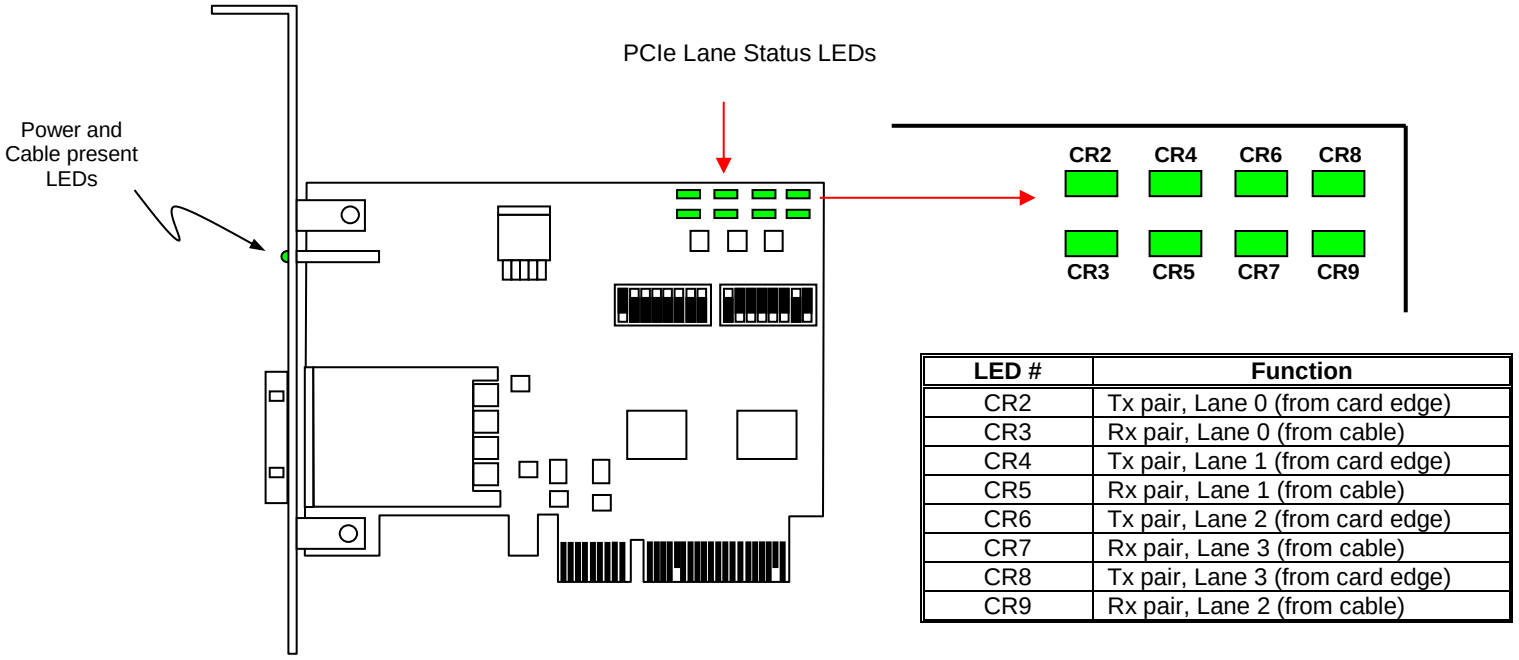


3.c. Installation instructions for a 2-slot backplane

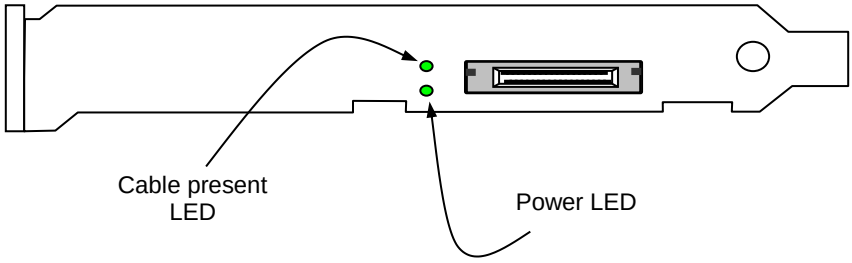
1) Insert the HIB2 x4 in host mode in a PCIe slot in the host computer
2) Connect the 2-slot backplane to an ATX power supply separate from the host system power supply.
3) Insert the HIB2 x4 in target mode in the PCIe connector on the test backplane, next to the ATX connector.
4) Insert the PCIe endpoint board in the other PCIe slot on the test backplane.
5) Connect the PCIe cable to both the host and target HIB2 x4.
6) Turn on the power supply for the test backplane. NOTE: The power supply and test backplane will not power up at this time.
7) Turn on the host system. Signals across the PCIe cable will cause the test backplane to power up as well. The power and cable LEDS on both HIB2 x4s should be on, indicating that the host system is communicating with the endpoint board.

4. Technical Information

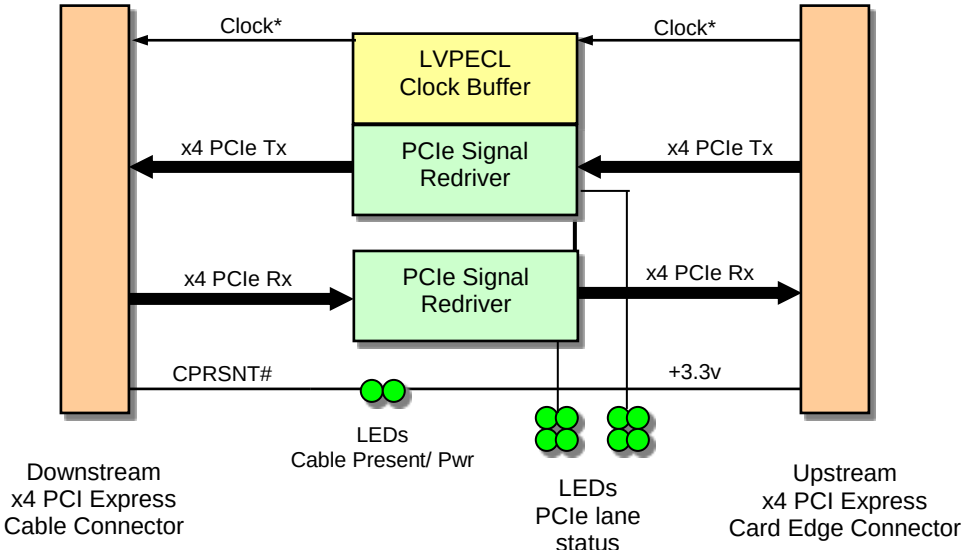
4.a. LEDs



LED #	Function
CR2	Tx pair, Lane 0 (from card edge)
CR3	Rx pair, Lane 0 (from cable)
CR4	Tx pair, Lane 1 (from card edge)
CR5	Rx pair, Lane 1 (from cable)
CR6	Tx pair, Lane 2 (from card edge)
CR7	Rx pair, Lane 3 (from cable)
CR8	Tx pair, Lane 3 (from card edge)
CR9	Rx pair, Lane 2 (from cable)



4.b. Block Diagram



*Clock direction shown in Host configuration

4.c. Pin Assignments

Connectors PCIe x4 Card Edge Connector

- The pins are numbered as shown with side A on the top of the centerline on the solder side of the board and side B on the bottom of the centerline on the component side of the board.
- The PCIe interface pins PETpx, PETnx, PERpx, and PERnx are named with the following convention: “PE” stands for PCIe high speed, “T” for Transmitter, “R” for Receiver, “p” for positive (+), and “n” for negative (-).
- Note that adjacent differential pairs are separated by two ground pins to manage the connector crosstalk.

Table 1: Pin-out for the PCIe x4 Card Edge Connector on the Host Cable Adapter

Pin #	Side B		Side A	
	Name	**Description**	**Name**	**Description**
1	N/C	N/C	PRSNT1#	Hot-Plug presence detect
2	N/C	N/C	N/C	N/C
3	N/C	N/C	N/C	N/C
4	GND	Ground	GND	Ground
5	NC	N/C	N/C	Not connected
6	N/C	N/C	JTAG3	Host Mode:TDI (Test Data Input) Target Mode: Test Clock+
7	GND	Ground	JTAG4	Host Mode: TDO (Test Data Output) Target Mode: Test Clock-
8	+3.3V	3.3 V power	N/C	Not connected
9	N/C	Host Mode: Not connected Target Mode: Test Power On	N/C	Not connected
10	3.3Vaux	3.3 V auxiliary power	+3.3V	3.3 V power
11	N/C	N/C	PERST#	Fundamental reset
Mechanical key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential pair, Lane 1	RSVD	Reserved
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2
26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	RSVD	Reserved	PERn3	
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved

PCI Table 2: Pin-out for the External PCIe Cable Connector

PIN #	Signal	Description	Notes
A1	GND	Ground reference for PCI Express transmitter Lanes	
A2	PETp0	Differential PCI Express transmitter Lane 0 5	5
A3	PETn0	Differential PCI Express transmitter Lane 0 5	5
A4	GND	GND Ground reference for PCI Express transmitter Lanes	
A5	PETp1	Differential PCI Express transmitter Lane 1 5	5
A6	PETn1	Differential PCI Express transmitter Lane 1	5
A7	GND	Ground reference for PCI Express transmitter Lanes	
A8	PETp2	Differential PCI Express transmitter Lane 2	5
A9	PETn2	Differential PCI Express transmitter Lane 2	5
A10	GND	Ground reference for PCI Express transmitter Lanes	
A11	PETp3	Differential PCI Express transmitter Lane 3	5
A12	PETn3	Differential PCI Express transmitter Lane 3	5
A13	GND	Ground reference for PCI Express transmitter Lanes	
A14	CREFCLK+	Differential 100MHz cable reference clock	
A15	CREFCLK	Differential 100MHz cable reference clock	
A16	GND	GND Ground reference for cable reference clock	
A17	SB_RTN	Signal return for single ended sideband signals	
A18	CPRSNT#	Used for detection of whether a cable is installed and the downstream subsystem is powered	
A19	CPWRON	Turns power on / off to slave-type downstream subsystems	
B1	GND	Ground reference for PCI Express receiver Lanes	
B2	PERp0	Differential PCI Express receiver Lane 0	5
B3	PERn0	Differential PCI Express receiver Lane 0	5
B4	GND	Ground reference for PCI Express receiver Lanes	
B5	PERp1	Differential PCI Express receiver Lane 1	5
B6	PERn1	Differential PCI Express receiver Lane 1	5
B7	GND	Ground reference for PCI Express receiver Lanes	
B8	PERp2	Differential PCI Express receiver Lane 2	5
B9	PERn2	Differential PCI Express receiver Lane 2	5

B10	GND	Ground reference for PCI Express receiver Lanes	
B11	PERp3	Differential PCI Express receiver Lane 3	5
B12	PERn3	Differential PCI Express receiver Lane 3	5
B13	GND	Ground reference for PCI Express receiver Lanes	
B14	PWR	+3.3VCable power	
B15	PWR	+3.3VCable Power	
B16	PWR RTN	Cable power return	
B17	PWR RTN	Cable power return	
B18	CWAKE#	Power management signal for wakeup events (optional)	1, 3
B19	CPERST#	Cable PERST#	

Notes:

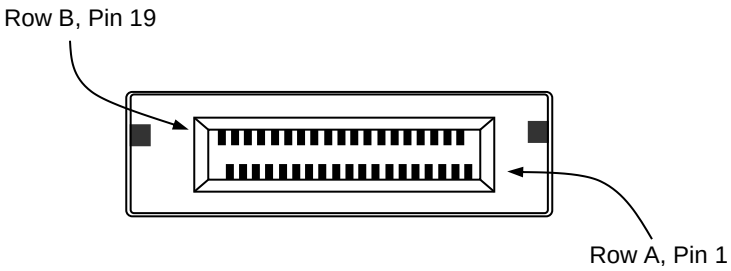
1 Optional signals that are not implemented are to be left as no connects on the board side connector.

2 Reserved signals must be left as no connects on the board side connector.

3 Although support of CWAKE# is optional from the board side connector perspective, an allocated wire is mandated for the cable assembly.

4 Board side pin-out on both sides of the Link is identical. The cable assembly incorporates a null modem for the PCIe transmit and receive pairs.

PCI Express x4 Connector Pin Assignment



PIN- out for the PCIe x4 Cable

Pin #	Cable Side 1		Cable Side 2	Pin #
A1 A4 A7 A10 A13 A16 B1 B4 B7 B10 B13	GND	Drain Wires	GND	A1 A4 A7 A10 A13 A16 B1 B4 B7 B10 B13
A2	PETp0	Differential Pair	PERp0	B2
A3	PETn0		PERn0	B3
A5	PETp1	Differential Pair	PERp1	B5
A6	PETn1		PERn1	B6

Pin #	Cable Side 1		Cable Side 2	Pin #
A8	PETp2	Differential Pair	PERp2	B8
A9	PETn2		PERn2	B9
A11	PETp3	Differential Pair	PERp3	B11
A12	PETn3		PERn3	B12
A14	CREFCLK+	Differential Pair	CREFCLK+	A14
A15	CREFCLK		CREFCLK-	A15
A17	SB_RTN	Hook-up Wire	SB_RTN	A17
A18	CPRSNT#	Hook-up Wire	CPRSNT#	A18
A19	CPWRON	Hook-up Wire	CPWRON	A19
B2	PERp0	Differential Pair	PETp0	A2
B3	PERn0		PETn0	A3
B5	PERp1	Differential Pair	PETp1	A5
B6	PERn1		PETn1	A6
B8	PERp2	Differential Pair	PETp2	A8
B9	PERn2		PETn2	A9
B11	PERp3	Differential Pair	PETp3	A11
B12	PERn3		PETn3	A12
B14	PWR	NC	PWR	B14
B15	PWR	NC	PWR	B15
B16	PWR_RTN	NC	PWR_RTN	B16
B17	PWR_RTN	NC	PWR_RTN	B17
B18	CWAKE#	Hook-up Wire	CWAKE#	B18
B19	CPERST#	Hook-up Wire	CPERST#	B19
Backshell	Chassis Ground	Overall Cable Braid	Chassis Ground	Back shell

4.d. Signal Descriptions

PETp(x)	PCI Express Transmit Positive signal of (x) pair.
PETn(x)	PCI Express Transmit Negative signal of (x) pair.
PERp(x)	PCI Express Receive Positive signal of (x) pair.
PERn(x)	PCI Express Receive Negative signal of (x) pair.
CREFCLK+/-	Cable REFerence CLocK: Provides a reference clock from the host system to the remote system.
SB_RTN	Side Band ReTurN: return path for single ended signals from remote systems.
CPRSNT#	Cable PReSeNT: Indicates the presence of a device beyond the cable.
PWR	PoWeR: Provides local power for in-cable redriver circuits. Only needed on long cables. Power does not go across the cable.)
PWR_RTN	PoWeR ReTurN: Provides local power return path for PWR pins.
CWAKE#	Cable WAKE
CPERST#	Cable PCI Express Reset

5. Ordering Information

OSS-KIT-EXP-4500